

TEES 2020

Model 2070LX +

TEES 2020 creates a Model 2070LX+ controller that meets all the requirements of the Model 2070LX controller. The Model 2070LX+ is designed to host multiple CPU boards. The multiple CPU Boards capability includes multiple Model 2070-1Es, Model 2070-ICs or a combination of both.

1.0 Hardware

1.1 Model 2070 LX+ Chassis

The Model 2070 Chassis has been redesigned for the Model 2070LX+. This new chassis adds three new plugs in slots, A6, A7 and A8. The network routing has been layout to accommodate network capabilities to all slots, A1, A2, A4, A5, A6, A7, A8. A3 does not contain network access since this slot is dedicated for the Field I/O and slot A8 is permanently dedicated for the Model 2070-LAN which is the core of the controller's Local Area Network (LAN).

1.2 Model 2070 LX+ Front Panel

The Model 2070LX+ Front Panel includes a network port. The front panel network port allows users to connect to the controller's LAN from an RJ45 Jack in the front panel. With the network RJ45 Jack in the front the panel the Model 2070LX+ contains two RJ45 Jacks, one for serial communications functionality and the second to for network communications.

1.3 Model 2070-LAN

The Model 2070LX includes a Model 2070-LAN network module the provides all network communications withing the controller. The Module 2070-LAN Module forms a Local Area Network between the plug-in modules in the slots within the controller and the switch in the Model 2070-LAN module. The Model 2070-LAN module an 8-port network switch, faceplate network traffic indicators for every port and a network access port (NAP).

1.4 Model 2070- 1C firmware

The Model 2070-1C is required to provides a bi-directional, asynchronous serial communications path from the Model 2070-1C CPU Module to microcontroller(s) in the Field I/O, and Front Panel. Firmware is included on the main processor of the CPU Module, and all microcontrollers, facilitating in-field firmware updates. As a minimum, the Field I/O processor and Front Panel processor are upgradeable via communications from the CPU Module.